

(19)



JAPANESE PATENT OFFICE

PATENT ABSTRACTS OF JAPAN

(11) Publication number: 04096358 A

(43) Date of publication of application: 27.03.92

(51) Int. Cl. H01L 25/065
 H01L 21/60
 H01L 23/28
 H01L 25/07
 H01L 25/18
 H05K 1/18

(21) Application number: 02211544

(71) Applicant: CASIO COMPUT CO LTD

(22) Date of filing: 13.08.90

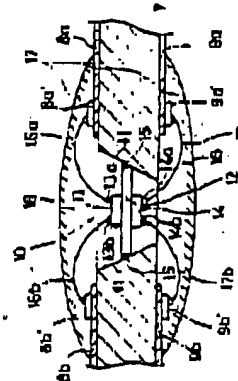
(72) Inventor: FUKUI YUICHI

(54) PRINTED WIRING BOARD

(57) Abstract:

PURPOSE: To load bare chips on a printed wiring board in thickness approximately equal to that of the printed wiring board, and to enable high density packaging by forming a pan-shaped hole in the printed wiring board and disposing the bare chips in the hole.

CONSTITUTION: A hole 10 such as having a pan shape is bored on a printed wiring board 7, to which pattern wirings are executed. A bare chip 13, 14 having integrated circuits are fitted on a surface/a rear of a mounting member 12 through bonding or sticking. The mounting member 12 is fixed on the inner circumferential surface of the hole. The chips are housed substantially within the board thickness of the printed wiring board 7. Pads 8a', 9a', 14a', 14b' formed on the chips and pads arranged on wiring patterns 8a, 8b, 9a, 9b are connected by wires 16a, 16b, 17a, 17b. The wires and the chips are coated with coating sections composed of spot coating materials 18, thus thinly constituting the layer thickness of coating materials. Accordingly, the bare chips can be mounted on both surfaces of the printed wiring board by sufficiently utilizing the thickness of the printed wiring board 7.



COPYRIGHT (C) 1992, JPO&Japio